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to create or evaluate designs targeting the Spartan®-6 XC6SLX16-2CSG324 FPGA. The SP601 provides board features for evaluating the Spartan-6 family that are common to most entry-level development environments.

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Summary The SP601 controller can be installed and Page
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guide describes the clocking resources available in all
Spartan-6 devices, including the DCMs and PLLs. †
Spartan-6 FPGA Block RAM Resources User Guide This guide
describes the Spartan-6 device block RAM capabilities.

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o Hardware User Guide – Detailed description of the SP601 Board features, jumper settings, options and pin location tables. o Reference Design User Guide – Step by Step guide on understanding, implementing, modifying and customizing the SP601 Reference Designs. o Board Design Files – Schematics/Gerbers/BOM •Cables & Power Supply.

Spartan-6 FPGA SP601 Evaluation Kit FAQ

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SP601 Setup. Connect a USB Mini-B Cable to the USB JTAG connector on the SP601 board. – Connect this cable to your PC. Compile MultiBoot Design. Unzip the rdf0006.zip file. Note: Presentation applies to the SP601. Compile MultiBoot Design. At a command prompt, type: cd sp601_multiboot run_all_build_script.bat.

XTP038: SP601 MultiBoot Design - Xilinx
Hardware User 's Manual NJ/NX-series CPU Unit Software
User 's Manual NJ/NX-series Instructions Reference
Manual NJ/NX-series CPU Unit Motion Control User's
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system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run. Reference Design IP.

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